REMARKS

The Office Action dated August 2, 2005, has been received and carefully noted. The following remarks are submitted as a full and complete response to the Office Action.

Claims 13 and 14 are amended to more particularly point out and distinctly claim the subject matter of the invention. Claim 16 is added. No new matter is added. Thus, claims 1-16 are pending in the subject application and are respectfully submitted for consideration.

Claim 13 was rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,760,341 (Erimli et al.). The Office Action took the position that Erimli taught each and every element of claim 13. Applicants respectfully submit that the cited reference fails to disclose or suggest all the features of any of the presently pending claims.

Claim 13, upon which claims 14 and 15 are dependent, recites a method for sharing memory between a first switch and a second switch connected to each other by an expansion bus. The method includes sending a command from a first switch to a second switch that the first switch is about to perform a memory read or write. The method also includes enabling data packets to be read or written to the first switch by the second switch through the expansion bus. The method also includes reading or writing a portion of packet data to local memory of the first switch using a memory bus. The method also

includes reading or writing another portion of packet data to alternate memory through the second switch using the expansion bus.

As discussed in the specification, examples of the present invention provide a switch having virtual shared memory. Examples of the present invention enable an expansion port to be provided on a switch to connect two switches together. Thus, two switches may read and write at a bandwidth of 128 Gbits/sec while maintaining a single memory bus master for each memory to reduce memory bus loading. Further, examples of the present invention may eliminate the need for two switches to be electrically connected to a centralized memory along a common bus. Thus, an electrical load may be decreased as compared to the use of a common bus. Applicants respectfully submit that Erimli fails to disclose or suggest all the elements of any of the presently pending claims. Therefore, the cited reference fails to provide the critical and unobvious advantages discussed above.

Erimli relates to the segmentation of buffer memories for shared frame data storage among multiple network switch modules. Each memory device is divided into memory segments, such that each memory segment is configured for storing frame data from a corresponding one of the switch modules. Switching logic 28 of Erimli forwards a frame pointer specifying the location of the received data packet to the other multiport switches 22 via an expansion port 30. Each of switch modules 22 include a memory interface 44 configured for controlling the storage of frame data in buffer memory devices 36 according to a prescribed protocol. Referring to Figure 2 of Erimli, bus 32

connects the switch modules and buffer memory devices together. Memory interfaces 44 assign memory segment A in each of buffer memory devices 36 to switching module 22a, memory segment B in each of buffer memory devices 36 to switching module 22b, and memory segment C in each of the buffer memory devices 36 to switching module 22c. Thus, switch module 22a can write frame data only into memory segment A of buffer memory devices 36a, 36b and 36c and so on. Each memory interface 44 can use a single frame pointer that specifies a specific memory address location and read frame data for a stored data frame from memory devices 36.

Applicants submit that Erimli fails to disclose or suggest all the features of claim 13. For example, Erimli fails to disclose or suggest enabling data packets to be read or written to the first switch by the second switch through the expansion bus. Erimli describes, for example, a switch module 22a sending the data frame to its buffer memory device 36 and forwarding the rest of the packet to other switches without directly accessing the other memory devices or using an expansion bus. Further, switch module 22a of Erimli fails to enable other switches from accessing its memory over an expansion bus.

In contrast, claim 13 recites "enabling data packets to be read or written to said first switch by said second switch through said expansion bus." Applicants maintain, for the reasons given above, that Erimli fails to disclose or suggest at least these features of claim 13. Thus, applicants respectfully request that the anticipation rejection be withdrawn.

Claims 1, 3-9, 11, 12, 14 and 15 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Erimli in view of U.S. Patent No. 6,011,793 (Smith). The Office Action took the position that Erimli taught all the elements of the claims except that "said expansion bus allows said first switch to directly access said second memory interface through said second switch and said second switch to directly access said first memory interface through said first switch to increase a bandwidth of a read/write operation to the first memory and the second memory." The Office Action then alleged that Smith provided the features of the claims missing from Erimli. Applicants respectfully traverse the obviousness rejection and submit that Erimli and Smith, either alone or in combination, fail to disclose or suggest all the features of any of the presently pending claims.

Claim 1, upon which claims 3-4 are dependent, recites a network of switches. The network includes a first switch having a first memory interface and a first expansion port. The network also includes a first memory coupled to the first switch with a first memory bus. The network also includes an expansion bus having a first expansion bus interface and a second expansion bus interface. The first expansion bus interface is connected to the first expansion port. The network of switches also includes a second switch having a second memory interface and a second expansion port. The second expansion port is connected to the second expansion bus interface, thereby connecting the first switch to the second switch. The network also includes a second memory coupled to the second switch with a second memory bus. The expansion bus allows the first switch to directly

access the second memory interface through the second switch and the second switch to directly access the first memory interface through the first switch to increase a bandwidth of a read/write operation to the first memory and the second memory.

Claim 5, upon which claims 6-8 are dependent, recites a switch for transmitting and receiving data packets. The switch includes a memory interface that accesses memory via a memory bus. The switch also includes an expansion port connected to the memory interface. The expansion port is configured to be connected to an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read/write operation.

Claim 9, upon which claims 11-12 are dependent, recites a system of network switches. The system includes a first switch having a first memory and a first expansion port. The system also includes an expansion bus having a first expansion bus end and a second expansion bus end. The first expansion bus end is connected to the first expansion port. The system also includes a second switch having a second memory and a second expansion port. The second expansion port is connected to the second expansion bus end, thereby connecting the first switch to the second switch. The expansion bus allows the first switch to directly access the second memory through the second switch and the second switch to directly access the first memory through the first switch to increase a bandwidth of a read/write operation to the first memory and the second memory.

Claims 14 and 15 depend from claim 13. Claim 13 is discussed above. Applicants submit that claims 14 and 15 include the features of claim 13, as well as other features.

Erimli is summarized above.

Smith relates to a switching apparatus for simultaneously switching a plurality of switch units, with each switch unit including storage regions corresponding to other switch units. Referring to Figure 3 of Smith, ATM switching apparatus 10 includes a plurality of switch units 20_0 to 20_2 and a control unit 30. Each switch unit includes a switch port management (SPM) portion 22 that is connected to the input port and output port of the switch unit, and also includes a memory portion 24. Each SPM portion 22 is connected to all three bus lines B_0 to B_2, while each memory portion 24 is only connected to one of the bus lines. Each memory portion 24 is divided into two storage regions corresponding respectively to the other switch units of the apparatus. In a first operating or writing phase, SPM portion 22 of switch unit 20 receives cells from its associated input port I. In response to receipt of each cell, SPM portion 22 writes the cell to the next consecutive free locations in the relevant storage region R of memory portion 24 in its own switch unit 20. For the reading phase, control unit 30 of the apparatus causes each SPM portion 22 to re-configure its bus selection so as to gain access to memory portions 24 in other switch units apart from its own. Thus, Smith describes plural switch unit-memory portion pairs being selected by the control unit for use in reading cell data, each pair having its own data transfer path using a different one of the bus lines B_0 to B_2.

Applicants submit that Erimli and Smith fail to disclose or suggest all the features of any of the presently pending claims. For example, Applicants submit that Erimli and Smith fail to disclose or suggest "said expansion bus allows said first switch to directly access said second memory interface through said second switch . . . to increase a bandwidth of a read/write operation to the first memory and the second memory," as recited in claim 1. Further, applicants submit that Erimli and Smith fail to disclose or suggest "an expansion bus connected to another switch thereby connecting two switches together allowing for sharing of memory to increase a bandwidth available for a read/write operation," as recited in claim 5. Claim 9 recites the patentable features of claim 1, as well as other features, but is drawn to a system of network of switches. With regard to claims 14 and 15, applicants submit that the cited reference does not disclose or suggest "reading or writing a portion of packet data to local memory of said first switching using a memory bus" and "reading or writing another portion of packet data to alternate memory through said second switch using said expansion bus," as recited in claim 13. Applicants respectfully submit that the cited reference does not disclose or suggest at least these features of the pending claims.

As noted above, Erimli fails to disclose or suggest all the features of claim 13. Applicants maintain that Erimli fails to disclose or suggest the features in the other claims listed above. Erimli fails to access two separate memories over an expansion bus and a memory bus. As shown in Erimli, bus 32 connects all the switch modules with each other and with the buffer memory devices. Erimli does not disclose or suggest a first

memory coupled to a first switch with a first memory bus, and a second memory coupled to a second switch with a second memory bus, and using an expansion bus to access the memories. By using two separate buses to perform, for example, a read/write operation, the bandwidth may be increased by the addition of the expansion bus in accessing the second memory. Erimli does not disclose or suggest this feature. Applicants also note that the Office Action confirms these distinctions between the claims and Erimli.

Applicants also submit that Smith, either alone or in combination with Erimli, fails to disclose or suggest the features of the claims missing from Smith. Smith describes switch units 20 having SPM portion 22 and memory portion 24. Each memory portion 24 is connected only to one of the bus lines. During different operations, SPM portion 22 and memory portion 24 of Smith use a different set of buses depending on the operation. As discussed with regard to the writing phase, Smith fails to disclose or suggest an expansion bus allowing the first switch to directly access the second memory interface and the second switch to directly access the first memory. Thus, Smith fails to use an expansion bus to allow the switches to directly access memories or memory interfaces. Further, with regard to the write phase, the switch unit 20 does not access a memory in another switch at all. Instead, Smith describes writing a cell to its own memory portion 24. As described in Smith, control unit 30 reconfigures the bus selection for SPM portion 22 to read from other switches. This reconfiguration is not in place for the write phase of Smith. Smith fails to disclose or suggest an expansion bus allowing a first switch to directly access a second memory through a second switch to increase a bandwidth of a

read/write operation to the first memory and the second memory as discussed above. Thus, Smith fails to disclose or suggest all the features of the presently pending claims.

The dependent claims are distinguishable from Erimli and Smith for the reasons given above, and also because they recite additional patentable subject matter. Thus, applicants maintain the Erimli and Smith, either alone or in combination, fails to disclose or suggest all the features of claims 1, 3-9, 11, 12, 14 and 15. Applicants respectfully request that the obviousness rejection be withdrawn.

The Office Action objected to claims 2 and 10. Applicants are grateful for the indication that these claims would be allowable if rewritten in independent form. However, Applicants submit that based at least on the above discussion regarding claims 1 and 9, these claims are allowable at least for the same reasons as claims 1 and 9. Accordingly, withdrawal of the objection to claims 2 and 10 is respectfully requested.

New claim 16 is added. Applicants respectfully submit that new claim 16 is allowable for the reasons given above and also because new claim 16 recites additional patentable subject matter.

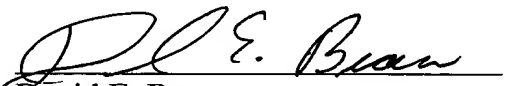
Applicants submit that each of claims 1, 3-9 and 11-16 recite subject matter that is neither disclosed nor suggested by the cited references. Therefore, applicants respectfully request that claims 1-16 be allowed and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by

telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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